

**Amendments to the Claims:**

This listing will replace all prior versions, and listing, of claims in the application.

1. (ORIGINAL) A method to improve solder bump reliability for interconnection of flip chip devices, comprising the steps of:

providing a substrate, at least one a contact pad having been provided over the surface of said substrate, a layer of passivation having been deposited over the surface of said substrate, said layer of passivation having been patterned and etched, exposing the surface of said at least one contact pad, a layer of Under Ball Metal (UBM) having been deposited over the surface of said layer of passivation including the exposed surface of said at least one contact pad;

creating at least one T-shaped layer of solder compound over the surface of said layer of UBM in at least one opening created in a layer of patterning material, said at least one T-shaped layer of solder compound being aligned with said at least one contact pad having been provided over the surface of said substrate;

removing said layer of patterning material, leaving in place said at least one T-shaped layer of solder compound, exposing the surface of said patterned layers UBM;

etching said exposed layer of UBM using said at least one T-shaped layer of solder compound as a mask; and

reflowing the surface of said solder compound, creating said solder bump.

Claims 2-28: (cancelled).

Please add the following new claims:

29. (NEW) A solder bump for interconnection of flip chip devices, comprising:

a substrate, active semiconductor devices having been created in or over said substrate;

at least one contact pad created over said substrate;

a patterned layer of passivation created over said substrate, said patterned layer of passivation exposing said at least one contact pad;

a patterned layer of Under-Bump-Metallurgy (UBM) created over said layer of passivation, including said at least one contact pad, a surface area of the patterned layer of UBM being limited to a size no larger than a size of a surface area of the at least one contact pad; and

at least one layer of reflowed solder compound overlying the patterned layer of UBM.

30. (NEW) The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

31. (NEW) The solder bump of claim 29, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

32. (NEW) The solder bump of claim 29, said patterned layer of passivation comprising a plurality of passivation layers.

33. (NEW) The solder bump of claim 32, wherein at least one of said plurality of passivation layers is PE  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$ , a photosensitive polyimide, phosphorous doped silicon dioxide or titanium nitride.

34. (NEW) The solder bump of claim 29, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

35. (NEW) The solder bump of claim 29, said at least one contact pad on said semiconductor substrate further comprising a contact

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pad formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

36. (NEW) The solder bump of claim 29, with a seed layer having been deposited over said patterned layer of passivation.